PATENT COOPERATION TREA[illegible]

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
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PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	10 August 2005 (10-08-2005)
Applicant's or agent's file reference PAT 2295W-90	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CA2005/000701	06 May 2005 (06-05-2005)	06 May 2004 (06-05-2004)

International Patent Classification (IPC) or both national classification and IPC
IPC(7): H01L 29/66, H01L 29/78, H01L 27/115, H01L 21/336, G11C 17/16

Applicant
SIDENSE CORP. ET AL

1. This opinion contains indications relating to the following items :

- [X] Box No. I — Basis of the opinion
- [ ] Box No. II — Priority
- [ ] Box No. III — Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV — Lack of unity of invention
- [X] Box No. V — Reasoned statement under Rule 43*bis*.1(a)(I) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI — Certain documents cited
- [ ] Box No. VII — Certain defects in the international application
- [X] Box No. VIII — Certain observations on the international application

2. **FURTHER ACTION**
If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later. (Nov 10/05)
(Mar 6/06) - entered go √ checked ISO
For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/CA	Date of completion of this opinion	Authorized officer
Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001(819)953-2476	09 June 2005 (09-06-2005)	Leah Smith (819) 956-9966

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   [X] the international application in the language in which it was filed

   [ ] a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of :

   a. type of material

      [ ] a sequence listing

      [ ] table(s) related to the sequence listing

   b. format of material

      [ ] on paper

      [ ] in electronic form

   c. time of filing/furnishing

      [ ] contained in the international application as filed.

      [ ] filed together with the international application in electronic form

      [ ] furnished subsequently to this Authority for the purposes of search.

3 [ ] In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statement that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments :

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(I) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	2-11, 13-17, 19-22, 24-35	YES
	Claims	1, 12, 18, 23	NO
Inventive step (IS)	Claims	2-11, 13-17, 21, 22, 25, 28, 29, 33-35	YES
	Claims	1, 12, 18-20, 23, 24, 26, 27, 30-32	NO
Industrial applicability (IA)	Claims	1-35	YES
	Claims	none	NO

2. Citations and explanations :

D1 - US 2003/0109090 A1 (Bertin et al) 12 June 2003
D2 - US 6,713,839 B2 (Madurawe) 30 March 2004
D3 - US 5,646,438 (Frerichs) 8 July 1997

D1 discloses forming a semiconductor structure (MOSFET or anti-fuse) having a dual thickness dielectric layer, the structure comprising a polysilicon gate (30) over a channel region in a substrate, a diffusion region (34) proximate to one end of the channel region, a variable thickness gate oxide (28) between the polysilicon gate and the substrate having an oxide breakdown zone fusible to form a conductive channel between the polysilicon gate and the channel region, a thicker portion of the variable thickness gate oxide being adjacent the diffusion region.

Claim 1 is not novel over of D1 (Article 33(2) PCT), D1 teaches all the features of claim 1. As such, claim 1 does not involve an inventive step.

Claim 2 appears to be novel and to involve an inventive step (Articles 33(2) and 33(3) PCT) since none of the prior art teaches or suggests a variable thickness gate oxide having a thick side on one end of the channel and a thin side at the other end of the channel wherein the thick and thin sides meet at a predetermined distance of the present length of the channel.

Claims 3-10 are considered novel and to involve an inventive step (Articles 33(2) and 33(3) PCT) since they depend on claim 2.

Claim 11 is considered novel and to involve an inventive step (Articles 33(2) and 33(3) PCT) since none of the prior art discloses an edge of the diffusion region and a portion of the polysilicon gate to be free of salicidation.

Claim 12 does not involve an inventive step over D1 (Article 33(3) PCT). Although D1 does not specifically disclose a memory array, it is commonly know in the art to (as seen from the background of the invention) that anti-fuses are used to form memory arrays.

Claim 13 appears to be novel and to involve an inventive step (Articles 33(2) and 33(3) PCT) since none of the prior art teaches or suggests a variable thickness gate oxide having a thick side on one end of the channel and a thin side at the other end of the channel wherein the thick and thin sides meet at a predetermined distance of the present length of the channel.

Claims 13-17 are considered novel and to involve an inventive step (Articles 33(2) and 33(3) PCT) since they depend on claim 13.

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Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made :

Claims 1, 12 does not comply with Article 6 of the PCT. The expression "variable thickness gate oxide having an oxide breakdown zone fusible to form a conductive channel between the polysilicon gate and the channel region" is confusing, it is not clear what this means. In the description page 12, lines 12-16, it is clear that the variable thickness gate oxide has a thick side and a thin side. The thin gate oxide edge meeting one diffusion region defines a fusible edge where oxide breakdown can occur and the thick gate oxide edge meeting the other diffusion region defines an access edge where oxide breakdown cannot occur and current can flow between the gate and diffusion region.

Claims 27 and 32 are identical and therefore claim 32 is redundant and should be removed.

The description does not comply with Article 5 of the PCT. As a patent document should be self contained, subject matter should not be incorporated by reference. Therefore the expression on page 1, line 4 which incorporates by reference should be removed

Every document in the description must be easily retrievable by the public, therefore the document on page 1, lines 3-4 should be replaced with its equivalent patent or publication number, or removed.

The patent number is missing in line 1 of page 4.

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of: V

Claim 18 is not novel and does not involve an inventive step over D2 (Articles 33(2) and 33(3) PCT). D2 discloses a method of forming a gate oxide of variable thickness for an anti-fuse transistor comprising the steps of growing an intermediate oxide in the channel region of the anti-fuse transistor (col. 2, line65 to col. 3, line 1), removing the intermediate oxide from a thin oxide region of the channel (col. 3, lines 1-2), and growing a thin oxide over the thin oxide region and the intermediate oxide in the channel region (col. 3, lines 2-6).

Claim 19 is not novel and does not involve an inventive step over D2 (Articles 33(2) and 33(3) PCT). D2 discloses forming a common gate over the two oxide regions (col. 4, lines 15-17).

Claim 20 does not involve an inventive step over D2 in light of D1 (Article 33(3) PCT). D1 discloses forming a diffusion region adjacent the intermediate oxide.

Claim 21 appears to be novel and involve and inventive step (Articles 33(2) and 33(3) PCT) since none of the prior art discloses forming a floating diffusion region adjacent the thin oxide region.

Claim 22 appears to be novel and involve and inventive step (Articles 33(2) and 33(3) PCT) since none of the prior art discloses selectively growing a salicidation protect oxide over the diffusion region.

Claim 23 is not novel and does not involve an inventive step over D3 (Articles 33(2) and 33(3) PCT). D3 discloses an anti-fuse transistor formed on a semiconductor material comprising an active area, a polysilicon gate (16) over the active area defining a fusible edge and an access edge, a thick gate oxide (22) adjacent the access edge, a diffusion region adjacent the access edge (12), a thin gate oxide adjacent the fusible edge (20), the thin gate oxide having lower breakdown voltage than the thick gate oxide for forming a conductive channel between the polysilicon gate and the diffusion region (col. 2, lines 25-43).

Claim 24 does not appear to involve an inventive step (Article 33(3) PCT) since making one edge longer than the other is within the skill of a person skilled in the art.

Claim 25 appears to be novel and involve an inventive step (Article 33(2) and 33(3) PCT) since none of the prior art discloses a length of the fusible edge being defined by at least two line segments of the polysilicon gate being at an angle to each other.

Claim 26 does not appear to involve an inventive step (Article 33(3) PCT) since defining the fusible edge by a width of the active area is within the skill of a person skilled in the art.

Claim 27 does not involve an inventive step over D3 in light if D1 (Article 33(3) PCT). D1 discloses a channel region between the fusible edge and the access edge, and the thick and thin gate oxides are disposed between the channel region and the gate.

Claim 28 appears to be novel and to involve an inventive step (Articles 33(2) and 33(3) PCT) since none of the prior art teaches or suggests a variable thickness gate oxide having a thick side on one end of the channel and a thin side at the other end of the channel wherein the thick and thin sides meet at a predetermined distance of the present length of the channel.

Claim 29 appears to be novel and to involve an inventive step (Articles 33(2) and 33(3) PCT) since it depends on claim 28.

Claims 30 and 31 are not considered to involve an inventive step (Article 33(3) PCT) since these features are within the skill of a person skilled in the art.

Claim 32 is identical to claim 27.

Claim 33 appears to be novel and involve and inventive step (Articles 33(2) and 33(3) PCT) since none of the prior art discloses forming a floating diffusion region adjacent the thin oxide region.

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Supplemental Box

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Continuation of: Supplemental Box

Claim34 appears to be novel and to involve an inventive step (Articles 33(2) and 33(3) PCT) since none of the prior art teaches or suggests a variable thickness gate oxide having a thick side on one end of the channel and a thin side at the other end of the channel wherein the thick and thin sides meet at a predetermined distance of the present length of the channel.

Claim 35 is considered novel and to involve an inventive step (Articles 33(2) and 33(3) PCT) since none of the prior art discloses an edge of the diffusion region and a portion of the polysilicon gate to be free of salicidation.

Claims 1-35 have industrial applicability (Article 33(4) PCT).